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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,753	01/07/2002	Timothy J. Fennell	10559-608001 / P12892	3204

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,753	FENNELL ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 April 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The corrected formal drawings were received on 4/18/2002. These drawings are acceptable.

Specification

2. The abstract of the disclosure is objected to because –, and– (coma) should be inserted after "database" (line 3) for proper grammar and for greater clarification. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. **Claims 2-22** are objected to because of the following informalities:

As per **claim 2**, –,– (coma) should be inserted after "claim 1" (line 1) for further clarity; –second simulation– should be inserted before "model" (line 3) to clearly identify that the model refers to the second simulation model and not the first simulation model.

As per **claim 3**, –,– (coma)) should be inserted after "claim 2" (line 1) for further clarity; "simulator" (line 2) should be –simulation– for proper antecedent basis; the claim is also objected to for incorporating the above error into the claim by claim dependency.

As per **claim 4**, –,– (coma) should be inserted after "claim 1" (line 1) for further clarity ; "the simulation model" (line 1) should be –each simulation model–for greater clarity since there are two models recited in claim 1, from the claim depends.

As per **claim 5**, "to be used" (line 8) should be deleted to clarify what is being claimed since the terms refer to intended use; "chip design response" (lines 8-9) should

be --response of a chip design-- for further clarification and to provide clear antecedent basis for "the chip design" recited in the claims 8 and 10.

As per **claim 6-8,10**, --,-- (coma) should be inserted after "claim 5" (line 1), "claim 6" (line 1), "claim 7" (line 1), "claim 5" (line 1), respectively for further clarity.

As per **claim 9**, --,-- (coma) should be inserted after "claim 5" (line 1) for further clarity; "describing a second simulator model" (lines 1-2) should be --said causing the instructions-- to provide for proper antecedent basis.

As per **claim 6-10**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 11**, --user interface-- should be inserted before "instructions" (line 10) to distinguish the user interface instructions from instructions recited on line 2 of the claim; "chip design response" (lines 10-11) should be --response of a chip design-- for further clarification and to provide clear antecedent basis for "the chip design" recited in the claims 14 and 16.

As per **claim 15**, "the simulation" (line 2) should be --a simulation-- for proper antecedent basis.

As per **claims 12-16**, --,-- (coma) should be inserted before "wherein" for further clarity; the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 17**, --user interface-- should be inserted before "instructions" (line 9) to clearly distinguish the user interface instructions from the instructions recited on line 2 of the claim; "chip design response" (line 9) should be --response of a chip

design-- for further clarification and to provide clear antecedent basis for "the chip design" recited in the claims 20 and 21.

As per **claims 18-22**, --,-- (coma) should be inserted before "wherein" for further clarity; the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-22** are rejected under 35 U.S.C. 102(e) as being anticipated by **Choi et al.** (US Patent Application Publication No. US 2003/0004699 A1).

As per **claims 1-2**, all of the elements of the claims are illustrated in Fig. 1 and further described in paragraph [0017] (page 1) to paragraph [0020] (page 2), wherein the representation of the simulation model is presented or described to the graphical user interface (GUI) as described in paragraph [0020] in the form of hardware descriptions (i.e., hardware description language code) which are necessarily stored in

some sort of database or file at least in system 100 in order for the user to perform selection of the representation (i.e., presentation) of the models from the list of at least the pre-designed IC models (see paragraph [0019]), wherein the receiving of the response of the simulation in response to the signal (i.e., test stimuli, appropriate input) applied to the desired model (i.e., first or second or any desired model selected for simulation response) is further taught in paragraph [0022], and wherein since the "model" being presented or described to the GUI also refers to models as well as systems and components (paragraph [0018]), the first, second and/or any subsequent models are accordingly included as part of these models and models selection/testing.

As per **claim 3,** all of the elements of the claim are described in the rejection of claims 1-2 above, from which the claim depends, wherein the further changing of the hardware descriptions stored in the database as part of the describing of the second simulation model is also part of the presentation of the component or model representation to the user via the GUI since a change in the model presentation would necessarily also require a change in the corresponding HDL code being presented or described (see [0020]) because otherwise simulation model and the representation of the simulation model (i.e., in HDL code) being described to the GUI would not be the same. This further changing of hardware descriptions is also part of the modification of the IC model as described in paragraph [0052], page 4, which would necessarily results in the changing of the hardware descriptions (i.e., HDL codes) in order to maintain the same representation of the model being presented to the user (paragraph [0020]).

As per **claim 4**, all of the elements of the claim are described in the rejection of claim 1 above, from which the claim depends, wherein further limitation in which the simulation model representing a processor chip is also taught in paragraph [0020], first sentence.

As per **claims 5,11,17,** the associating (i.e., corresponding) of the functional processes (i.e., functions and responses) which are then executed/implemented in the simulation model(s) or modeler is described in paragraph [0020], page 2, (see also paragraph [0018], page 2) which are necessarily stored in some sort of database or file at least in system 100 in order for the user to perform selection of the representation (i.e., presentation) of the models from the list of at least the pre-designed IC models (see paragraph [0019]), wherein associating the graphical user interface (GUI) instructions and causing/using the instructions to simulate the chip design response is further described in paragraph [0022] wherein the user selection/provision of the particular test(s) to be simulated provides for the instructions associated with the GUI for simulation, wherein the processor, memory, computer-readable medium, instructions, computer system is further described in paragraph [0057], page 5 (see also Fig. 2).

As per **claims 6-8,12-14,18-20**, all of the elements of the claim are described in the rejection of claims 5,11,17 above, from which the claims respectively depend, wherein the various hierarchical relationships or connections being coupled and combined, and/or repetitively combined as defined in Applicant's specification, page 4, lines 5-15, correspond to the hierarchical relationships as illustrated in Figs. 5 and 6

(see also paragraph [0043]) in which the user is allowed to combined various existing components and/or user customized components (paragraphs [0019], [0050], [0052] until a final design or chip design is finalized.

As per **claims 9,15,21**, all of the elements of the claim are described in the rejection of claims 5,11,17 above, from which the claims respectively depend, wherein the further changing of the hardware descriptions stored in the database as part of the describing of the second simulation model is also part of the presentation of the component or model representation to the user via the GUI since a change in the model presentation would necessarily also require a change in the corresponding HDL code being presented or described (see [0020]) because otherwise simulation model and the representation of the simulation model (i.e., in HDL code) being described to the GUI would not be the same. This further changing of hardware descriptions is also part of the modification of the IC model as described in paragraph [0052], page 4, which would necessarily results in the changing of the hardware descriptions (i.e., HDL codes) in order to maintain the same representation of the model being presented to the user (paragraph [0020]).

As per **claims 10,16,22**, all of the elements of the claim are described in the rejection of claims 5,11,17 above, from which the claims respectively depend, wherein further limitation that chip design represents a process chip is also taught in paragraph [0020], page 2, first sentence.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 703-306-3039. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(703) 746-4111 (for informal or draft communications, please label

"PROPOSED" or "DRAFT" and let the examiner know prior to faxing) Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

8. **Applicant should note that effective May 1, 2003, the United States Patent and Trademark Office has a new Commissioner for Patents address for transitioning to the new Office location in Alexandria, VA, wherein correspondence in patent-related matters to organizations reporting to the Commissioner for Patents must now be addressed to:**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PK
December 14, 2003

PHALLAKA KIK
U.S. PATENT EXAMINER